

## Digital Group

The ISD Digital Systems Group designs and develops state-of-the-art, efficient and high-quality digital hardware systems. Its core abilities include: System Definition, Design & Development, Validation, RTL to Gate and Prototyping.

### System Definition

ISD's System Architects provide reliable systems starting from a general concept, an industry standard or a software algorithm. They establish the hardware/software partitioning, create a full system definition and define the hardware architecture, providing accurate documentation.

### Design & Development

ISD designs and develops full hardware systems by using the VHDL and Verilog hardware description languages and thoroughly documenting the implementation process. The hardware development is targeted to be efficient, reliable and reusable. The ISD Designers areas of expertise include video processing, network physical layers, on-chip and off-chip protocols, multi-clock synchronization issues and complex arithmetic functions. ISD has designed extensive parts of several Systems on a Chip (SoCs), such as video processing pipelines, DMA engines, communication protocol controllers, audio processing blocks, resynchronization engines, bus mastering devices, etc.

### Validation

All the hardware that is developed by ISD is exhaustively validated to ensure its reliability. The validation process is defined, documented and executed until the proper operation can be guaranteed. ISD is also involved in Design For Test architectures, modeling for verification purposes and in-house verification tools development. In all the systems and parts of systems ISD has contributed, ISD was fully involved in validating the hardware. Part of the validation has been performed on Aptix and Celaro platforms. For many of the System on Chip parts, we have also developed C models for validation purposes. ISD has created two in-house tools for the verification process: a generic program-based test-bench designed for complex simulation scenarios and an FPGA module program-based test-bench which targets seamless simulation and on-board testing for prototype boards. The generic program -based testbench is synthesizable for direct use on Aptix and Celaro platforms.

### RTL to Gate

ISD is involved in the RTL-to-Gate process by being able to perform RTL synthesis, timing analysis, formal proof and ATPG test coverage analysis for ASICs as well as vendor-specific RTL-to-Gate processes for ASIC and FPGAs. ISD has also the capacity to execute the whole backend ASIC flow.

### Prototyping

The Prototyping activity defines, designs, develops and tests Printed Circuit Boards (PCBs) which facilitate FPGA prototyping for system validation.